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Specification and Drawings as originally filed, with Application for Patent Serial No: **2,279,774,** on August 9, 1999, by **DATARADIO INC.,** assignee of Richard Vallée, André Beaudin and Michel Martin, for " Spacial Diversity Radio Receiver ".

Agent certificateur/Certifying Officer

February 26, 2004

Date

ABSTRACT

A spatial diversity radio for receiving and evaluating data in the form of a stream of symbols includes multiple receivers having spaced-apart antennae, each receiver comprising a circuit providing both a signal indicative of received signal strength and a demodulated signal output, a circuit to evaluate the signals indicating received signal strength, and generating control signals responsive thereto, a circuit combining the demodulated signal outputs in proportions controlled by said control signals to provide a combined output signal, and a circuit evaluating successive symbols represented by the combined output signal. Typically, signals above a threshold level and differing in strength by less than 6dB are linearly combined according to their relative strength, signals more than 6dB below the strongest signal are ignored, signals below threshold level are averaged, if no stronger signal is available, and rapidly-fading signals are excluded, if a non-fading signal is available.

TITLE: SPATIAL DIVERSITY RADIO RECEIVER

FIELD OF THE INVENTION

This invention relates to spatial diversity radio receivers, particularly for data signals.

BACKGROUND OF THE INVENTION

Land mobile radio systems as used for dispatch applications use frequency modulation which has proven to be well suited to the application by reason of immunity to impulse noise common in the vehicular environment. More recently, such systems have been required to transmit data as well as analog speech. Recent advances in computer technology have increased the demand for higher bit rates for data transfer.

Radio frequencies are regulated. While demands for higher bit rates are wide spread, regulatory agencies have not increased the bandwidth needed to facilitate high speed data transmission. In fact, the trend is in the opposite direction. In 1997 the Federal Communications Commission mandated the use of channels which are one half or one quarter as wide as those previously authorized. As taught by Shannon and Nyquist, there is a proven relationship between the bit rate of a channel, the bandwidth of the channel and the signal to noise ratio required to decode the data accurately. As the bit rate increases, all else being equal, the signal to noise ratio required to decode the data is also increased, and thus the range of the radio system is reduced as the bit rate increases.

Land mobile channels differ from those used in fixed microwave point to point services and satellite systems by virtue of reflections and fading of the signals. Signals arriving at or from a moving vehicle are almost always comprised of a complex amalgam of waves, some directly from the sending antenna and other reflected from stationary and moving objects. In the worst case scenario. The total received signal is composed of reflected signals. The resulting waveform caused by the combination of reflected signals (worse case)

and/or direct signal plus reflected signals, is subject to cancellation or reinforcement in the amplitude domain as well as distortion in the time domain resulting from propagation delays over the varying length paths taken by reflected signals. Both the amplitude and time distortions make decoding of the signals more difficult. It is not uncommon for cancellation to reduce the incoming signal to a level far below the threshold required for reliable decoding by the receiver. This effect is referred to as multi-path fading.

In data systems, such cancellations or "drop outs" erase portions of the desired bit stream. The duration of the erasure is a function of the average signal strength, the wavelength of the radio signal, the speed of the vehicle and that of moving reflectors in the vicinity. Forward Error Correction (FEC) is a common technique for solving this erasure problem. Redundant information is added to the transmitted data to allow for a predicted level of erasures and recovery of the original data without retransmission. FEC is useful but as the bit rate increases, more and more redundancy must be added which leads to diminishing returns. The redundancy reduces the effective bit rate of the system.

Another solution to problems caused by multi-path fading is to increase the complexity of the receiving system. Fading can be mitigated by using multiple receivers and multiple antennas. Such systems are often called diversity receivers since they are based on spatial diversity. Two or more receivers with separate antennae spaced an appropriate distance apart from each other give rise to probabilities that destructive interference experienced at one antenna may not be present on others.

Spatial diversity receiving systems conventionally use signal strength information to select the single best signal available. Information from the alternate receivers is ignored.

Such systems are often called "switching" or "switched combining" systems. Their weakness is that they ignore additional information present in

the streams produced by alternate receivers. Using a more intelligent system which extracts the maximum possible information content from all the receivers yields better performance.

One such system is exemplified by U.S. Patents Nos. 5,499,272 (Bottomley) and 5,701,333 (Okanowe et al) in which data is derived from the received channels to estimate and accumulate received data sequences, thus producing a synthesized received data stream. U.S. Patent No. 5,862,192 (Huzsar et al) compares received sample sequences for multiple channels with sequences corresponding to particular symbol sequences, and selects sample sequences on the basis of this comparison. U.S. Patent No. 5,901,174 (Joe 1) applies weightings to the received channels desired from both of a channel estimate and a global estimate of the signal. Another system, described in U.S. Patent No. 5,640,695 (Fitzgerald), uses a more sophisticated switched combination system. U.S. Patent No. 4,972,434 (Le Polozec et al) has an adaptive equalizer in each channel to derive a distortion factor for that channel which is used to weight signal strength measurements used by a combiner to select a received channel.

SUMMARY OF THE INVENTION

We process signals from multiple receivers in parallel to provide, for each receiver, analog signals representing both the received signal and a signal representing the strength of the received signal. Each of the received signals is sampled to produce a stream of digitized sample signals, and the sample signals from the different receivers are combined with weightings determined by the signal strength signals according to a predetermined set of evaluation rules, following which decisions are made as to the identity of symbols represented by the sample signals. The rules are selected to provide good data recovery based on combining the information content of the signals from the multiple receivers, it being understood that changes in the strength of the received signal at each receiver are part of this information content, the received signals from the receivers being combined wherever signal strength data suggests that such combination would be advantageous.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference will now be made to the accompanying drawings which show, by way of example, a presently preferred embodiment of the present invention, and in which:

Figure 1 is a schematic diagram of a first radio receiver;

Figure 2 is a schematic diagram of a second radio receiver having an antenna spaced from that of the first receiver;

Figure 3 is a schematic diagram of a digital signal processor implementing a digital data demodulator receiving signals from the first and second receivers; and

Figure 4 is a graph illustrating the combination of received signals.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figures 1 and 2, the receivers shown therein may be identical, and the same reference numerals are used to refer to the same parts. Only signals generated by the two receivers are differentiated by being designated with the suffixes 1 and 2 respectively. While a system utilising two receivers having spaced antennas is described, similar principles to those described below may be applied to systems employing three or more spaced antennas.

The receivers each comprise an antenna 2,an FM receiver 4 in turn comprising a radio frequency (RF) section 6, an intermediate frequency (IF) section 8, and a baseband section 10 which detects and regenerates a baseband signal. The IF sections 8 provide analog radio signal strength indicator (RSSI) signals RSSIA1 and RSSIA2 respectively, conveniently derived by summing stage currents in limiting amplifiers in each IF section, although other known techniques for deriving such signals may be utilised. In an exemplary embodiment, the IF sections are designed so that the RSSI signals exhibit a temperature stable monotonic logarithmic characteristic over a range of greater than 70 db.

The baseband section incorporates an FM detector circuit, typically a quadrature detector which splits the IF signal into two parts of which one part passes through a network with a phase shift of 90 degrees plus a shift proportional to the IF deviation from center frequency, while the other part passes straight through; multiplies the shifted and unshifted parts together; and selects the baseband frequency portion of the multiplier output spectrum to provide baseband analog signals RXA1 and RXA2

The signals RSSIA1, and RSSIA2, RXA1 and RXA2 are passed through respective 3-pole and 1-pole anti-aliasing filters 12 and 14 which limit their bandwidth to exclude noise and components at frequencies of more than half the sampling rate applied in analog to digital converters (ADC) 16 and 18, to which are passed the signals output from the filters 12 and 14. Typically, the ADCs 16 used to digitize the RSSI signals are sample and hold converter which track an analog input signal during a sample mode and hold it fixed during a hold mode to the instantaneous value of the signal at each transition from the sample to the hold mode. Typically, the ADCs 18 used to digitize the RXA signals to produce signals RXD1 and RXD2 are oversampling converters comprising an input signal conditioning circuit, a differential fifth order delta-sigma modulator, a 64X oversampling decimation circuit and a high pass filter from which output signals pass to a serial interface 26 (see Figure 3). A typical sampling rate for both converters 16 and 18 is at least 2.5 times the bit rate of the data being received, and in any case, greater than the Nyquist rate.

Referring now to Figure 3, the components shown therein are typically implemented by a digital signal processor (DSP) 20 suitably programmed to implement the illustrated signal processing functions, using techniques well known to those skilled in the art of DSP selection and programming.

The digitized inputs RXD1 and RXD2 are applied to an adaptive DC bias compensation filter 22 which compares their DC levels and develops a differential signal which is applied to one of the signals through an adder 24.

The difference signal is disabled whenever at least one RSSI signals falls below a threshold level. Its primary purpose is to compensate for differences in frequency, modulation level and other factors which may influence the DC bias levels of demodulated signals from the various channels that may be received. The adjusted RXD signals are then passed to a combination circuit in which they are multiplied in a ratio : $\alpha : 1 - \alpha$ in multipliers 26, 28 by the RSSI signals, which have previously been passed through digital filters 30, 32 and passed through circuits 34, 36 which adjust them to signals proportional to the dBm levels of the original RSSI signals, and evaluate them to provide control signals for the combiner circuit. The multipliers are only enabled when two RSSI signals to which they respond are both above a threshold level (for example - 123 dBm) below which reliable demodulation is not possible, and differ by less than 6dB. The RXD signals so adjusted (dBm (RXD1) and dBm (RXD2)) are summed by a combiner circuit 38 to provide a combined RXD signal according to the following expression, provided that the RSSI signals differ by less than 6dB:

$$\text{RXD combined} = \alpha.\text{RXD1} + (1 - \alpha).\text{RXD2}$$

where $0 \leq \alpha \leq 1$ and

$$\alpha = (0.5 + \text{dBm (RXD1)} - \text{dBm (RXD2)})/2.\text{skew}$$

where skew is < 6db.

The combiner is controlled to provide various different results according to RSSI values.

If there is more than one RSSI signal above the threshold at which the multipliers are operative, and the strengths of these signals differ by less than 6db, a linear combination of the RXD signals is effected according to the above expression. This results in a simple averaging of the adjusted RXD signals if the RSSI signals are equal.

If at least two of the RSSI signals rise above a much higher threshold (for example - 80 dBm), then the multipliers may be programmed to

cease to operate which results in a symmetrical averaging of the signals. A signal below the lower threshold is otherwise normally ignored.

A signal whose RSSI is more than 6db below that of the strongest signal is also normally ignored. We have found however that selection of a rapidly changing signal, whether fading or augmenting, tends to provide poor results, and such a signal should thus be ignored, if possible, even though its instantaneous strength is much greater than the other signal or signals unless, of course, every other signal suffers from the same problem. If, when tracked across several samples, the signal strength shows a rate of change approaching that associated with the bit rate of the data being transmitted, then the signal should not be utilised if a better signal is available. The exact threshold will depend on the radio frequency employed, as well as the bit rate of the data.

Figure 4 illustrates the operation of the combiner. The lower two graphs plot the outputs of the amplifiers 36 for two channels through successive samples, while the uppermost graph illustrates the proportions in which the RXA signals are combined by the combiner circuit 38 with 1 representing a combination entirely formed by the upper channel, and 0 representing a combination formed entirely by the lower channel. Thus along the time axis of the graphs, the signal of the lower channel from about 100 to 1100 is more than 6dB greater than that from the upper channel, so the latter alone is selected. At around 1700, both signals are above -80 dBm, and they are thus simply averaged. At about 2300, the signals differ by just less than 6 dB, with the upper channel greater, and a linearly apportioned output is taken, 0.9 from the upper channel at its peak value, and 0.1 from the lower channel. It should be noted that the combiner works on a symbol-by-symbol basis using symbol timing recovered during subsequent processing, and thus the operation of the combiner is controlled by the RSSI signals over the period of a symbol. If an RSSI level is changing excessively over the course of a symbol, this is an indication that the combination effected by the combiner circuit should exclude

the corresponding RX signal for that symbol, provided that another acceptable RX signal is available.

The output from the combiner circuit 38 is passed to a digital filter 40, and thence to a polyphase interpolation filter 42 whose purpose is to provide an accurate interpolation of an original signal produced by a Nyquist sampling process. It uses a over-sampling process to interpolate additional points to a curve reconstructing the original signal, using a sampling rate which varies according to the symbol rate, the sample rate of the converters 18, and the speed of the DSP. The oversampled signal reduces timing jitter, as compared to the Nyquist sampled signal, and enables more accurate recovery of symbol timing by a phase-locked loop 44 implemented by the DSP, which loop provides a timing output to an integrate and dump module 46 implemented by the DSP.

The output provided by the block 46 for each symbol 13 passed to a decision circuit 48 which evaluates the symbol, typically based upon a decision feedback method in which both the value of the output and the decisions made in respect of previous symbols are used to provide a most likely estimate of the symbol being decoded.

It will be noted that, in operation, the system continuously evaluates, in parallel, the signals received by each receiver utilised, and combines data from these signals such as to recover and combine information from each channel deemed able to contribute to correct evaluation of the received data. The evaluation tests and combination techniques described above are those presently believed to provide the best chance of correctly evaluating symbols of a data transmission, but these may be varied within the scope of the appended claims with a view either to improving performance, simplifying implementation, or taking advantage of improved DSP or other technology used to implement the digital circuits of the receiver. Although it is considered that use of a suitably programmed DSP is presently the optimum technology for implementing digital functions of the invention, other technology capable of implementing the same functions may, of course, be used. The

individual circuit functions and processing functions utilised in the receiver are, individually, well understood by those skilled in the art, and although particular implementations of these functions may have been described, it should be understood that functionally equivalent or superior implementations may be substituted. For example, it is believed that the above-noted unreliability of data recorded from rapidly-fading signals may be due to performance shortcomings of the discriminator utilised to demodulate the FM signal in block 10; substitution of an alternative demodulator providing improved performance under such circumstances is intended to be within the scope of the invention. Likewise, particular functions may be performed at different points in the system if functionally equivalent results are obtained. For example, the configuration of the digital circuits processing the received signal to evaluate signal strength parameter and combine the signals is exemplary only, and functionally equivalent implementations having a different distribution of functions may be used to combine the signals from the receivers in proportions determined by an evaluation of signal strength parameters such as dBm and rate of change of signal strength.

WHAT IS CLAIMED IS:

1. A spatial diversity radio receiver for receiving and evaluating data in the form of a stream of symbols, comprising multiple receivers having spaced-apart antennae, each receiver comprising a circuit providing both a signal indicative of received signal strength and a demodulated signal output, a circuit to evaluate the signals indicating received signal strength, and generating control signals responsive thereto, a circuit combining the demodulated signal outputs in proportions controlled by said control signals to provide a combined output signal, and a circuit evaluating successive symbols represented by the combined output signal.

2. A receiver according to Claim 1, wherein the circuit to evaluate the signals indicates received signal strength includes means to determine whether each received signal is above a threshold level, and the combining circuit is configured to exclude signals below the threshold level from the combined signal output.

3. A receiver according to Claim 1, wherein the combining circuit is configured to exclude from the combined signal output a signal weaker than the strongest signal by more than a predetermined margin.

4. A receiver according to claim 3, wherein the margin is 6dB.

5. A receiver according to Claim 3, wherein the combining circuit is configured to combine signals having a strength above the threshold level in proportion to the extent that they exceed a level set a predetermined margin below the strength of the strongest signal.

6. A received according to Claim 5, wherein the margin is 6dB.

7. A receiver according to Claim 1, wherein the circuit to evaluate the signals indicating received signal strength includes means to determine whether the

signal strength of each received signal is changing at a rate above a predetermined level, and the combining circuit is configured to exclude such a signal if another acceptable signal is available.

8. A receiver according to Claim 1, wherein the evaluation and combination circuits are digital, and further including an interpolation circuit processing said combined signal to provide a signal with reduced temporal jitter, a phase-locked loop receiving the signal provided by the interpolation circuit and locked to a symbol rate of the combined signal to provide symbol timing data, defining symbol periods, and a decision circuit receiving said combined signal and said timing data and deciding the value of successive symbols on the basis of the values of said combined signal during each symbol period and decisions as to the value of preceding symbols.

9. A receiver according to Claim 2, including an adaptive DC bias compensation circuit to adjust the relative DC levels of the received signals applied to the combination circuit when more than one signal above the threshold level is present.

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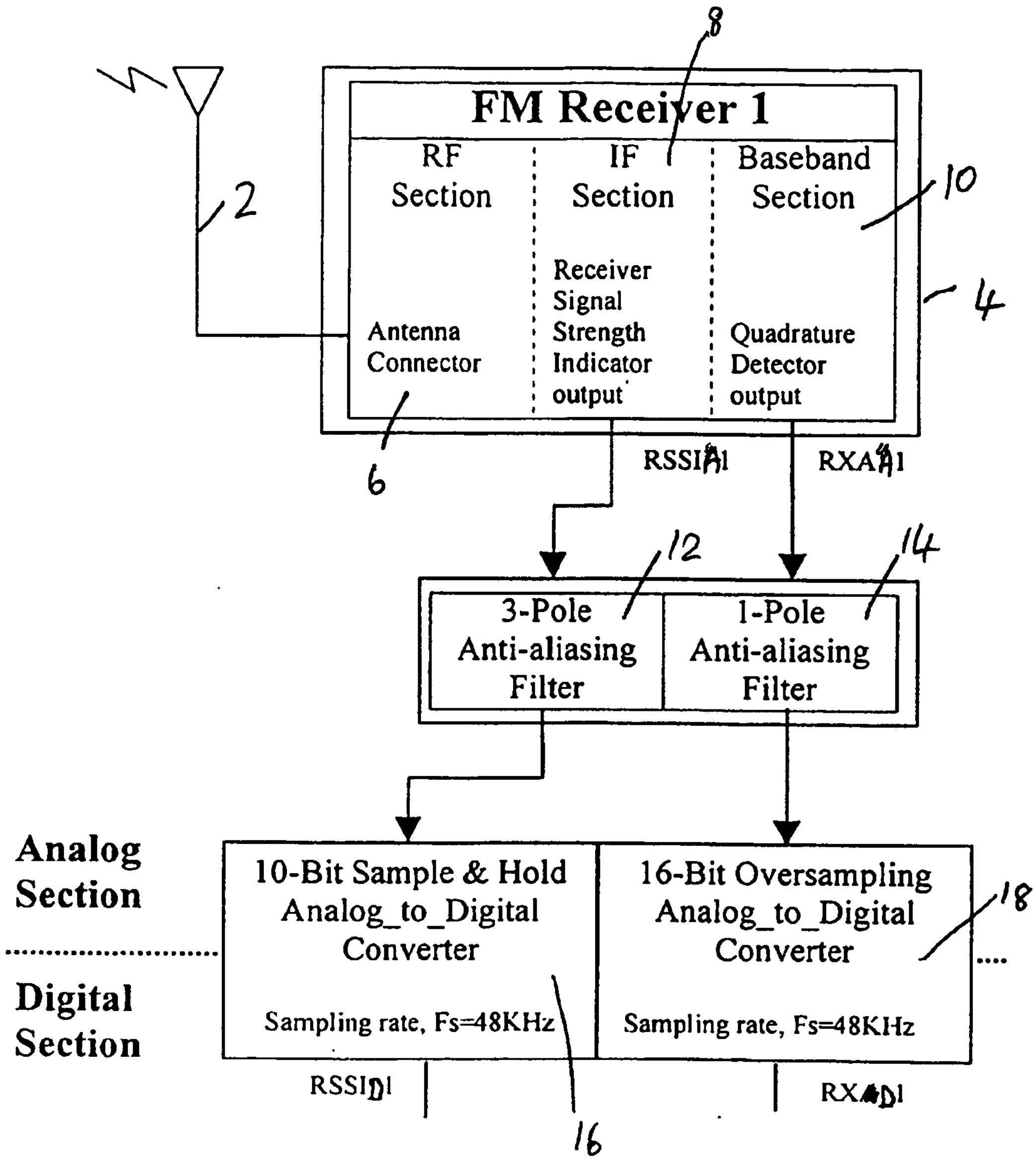

FM Receiver 1
RF Section
IF Section
Baseband Section
Antenna Connector
Receiver Signal Strength Indicator output
Quadrature Detector output
RSSIA1
RXAA1
3-Pole Anti-aliasing Filter
1-Pole Anti-aliasing Filter
Analog Section
Digital Section
10-Bit Sample & Hold Analog_to_Digital Converter
Sampling rate, Fs=48KHz
16-Bit Oversampling Analog_to_Digital Converter
Sampling rate, Fs=48KHz
RSSID1
RXAD1
2
4
6
8
10
12
14
16
18

Fig. 1

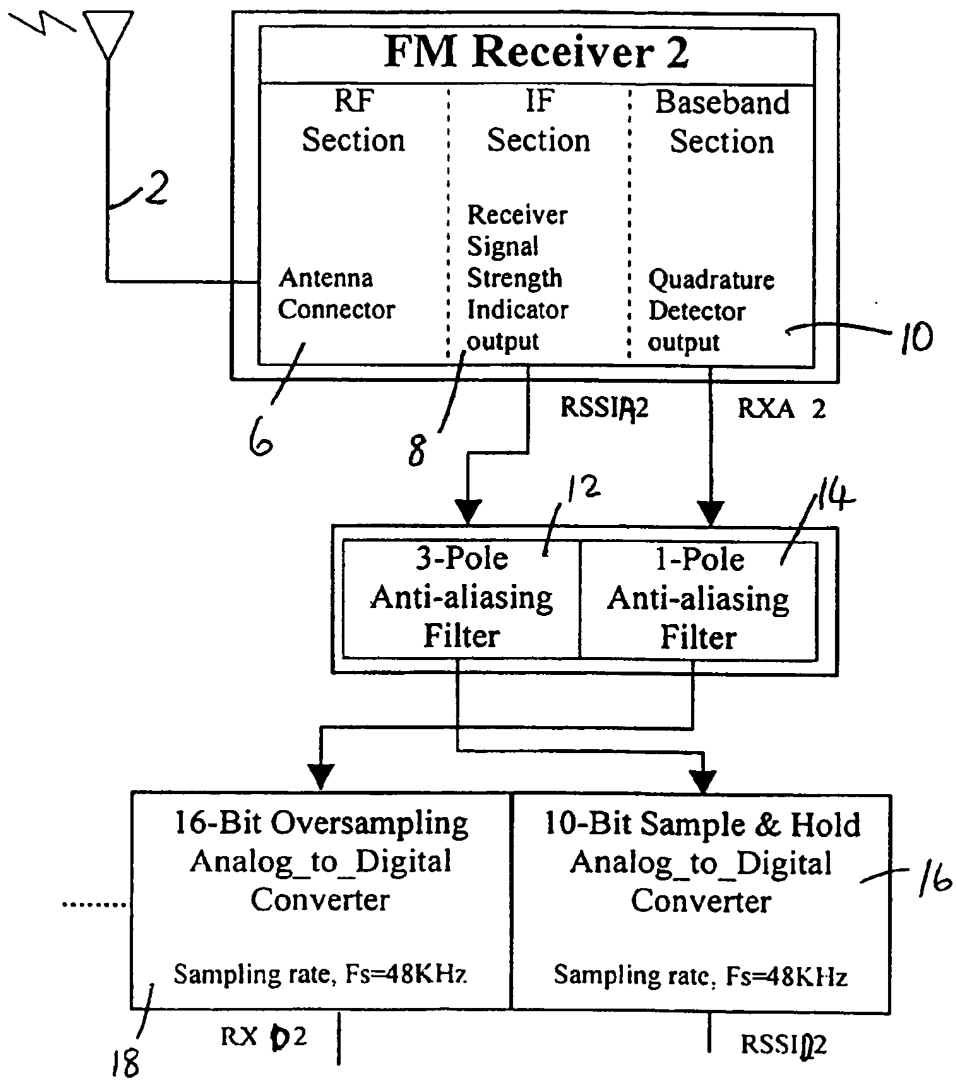

FM Receiver 2
RF Section
IF Section
Baseband Section
Receiver Signal Strength Indicator output
Antenna Connector
Quadrature Detector output
2
6
8
10
RSSIA2
RXA 2
12
14
3-Pole Anti-aliasing Filter
1-Pole Anti-aliasing Filter
16-Bit Oversampling Analog_to_Digital Converter
Sampling rate, Fs=48KHz
10-Bit Sample & Hold Analog_to_Digital Converter
Sampling rate, Fs=48KHz
16
18
RX D2
RSSID2

Fig. 2

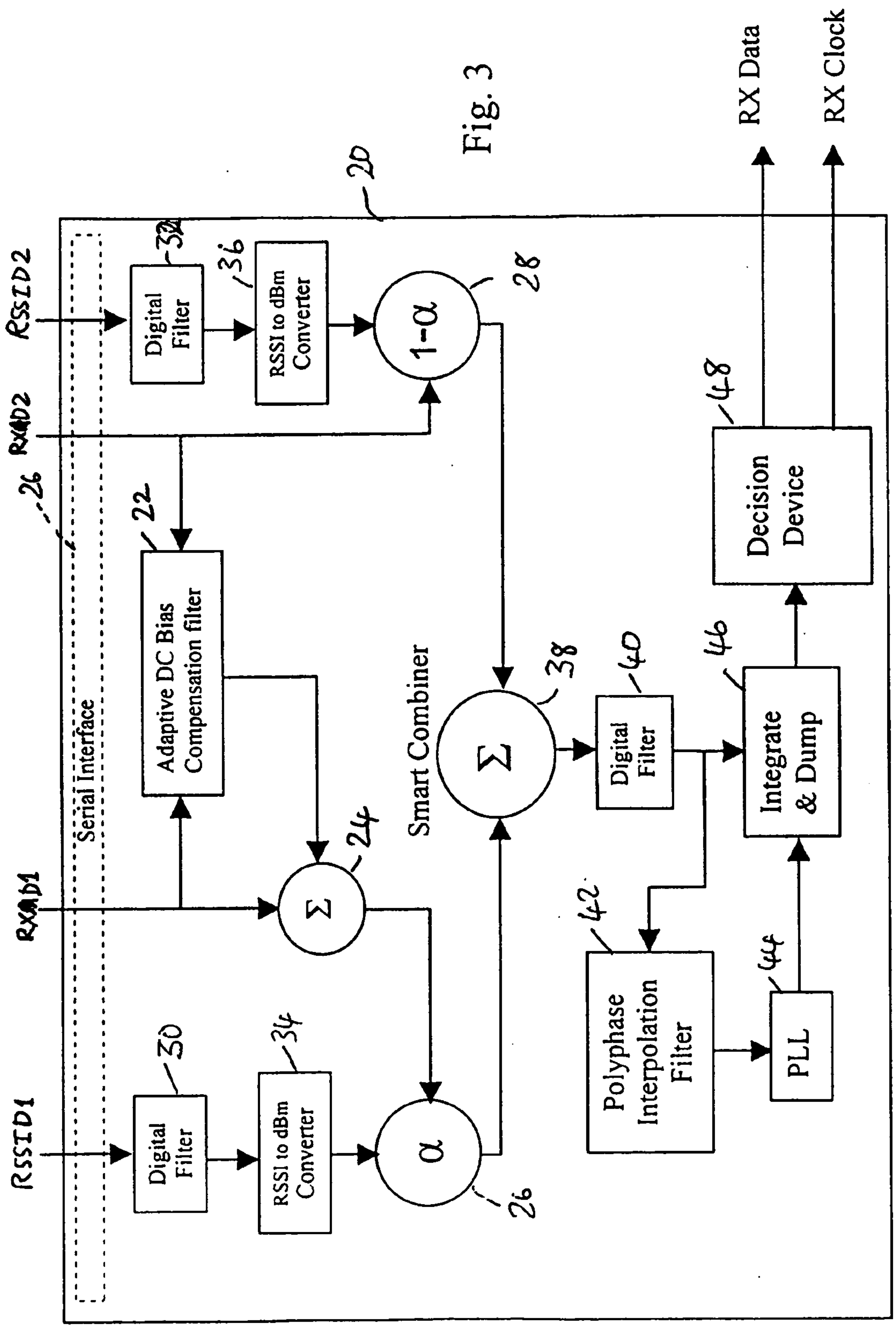
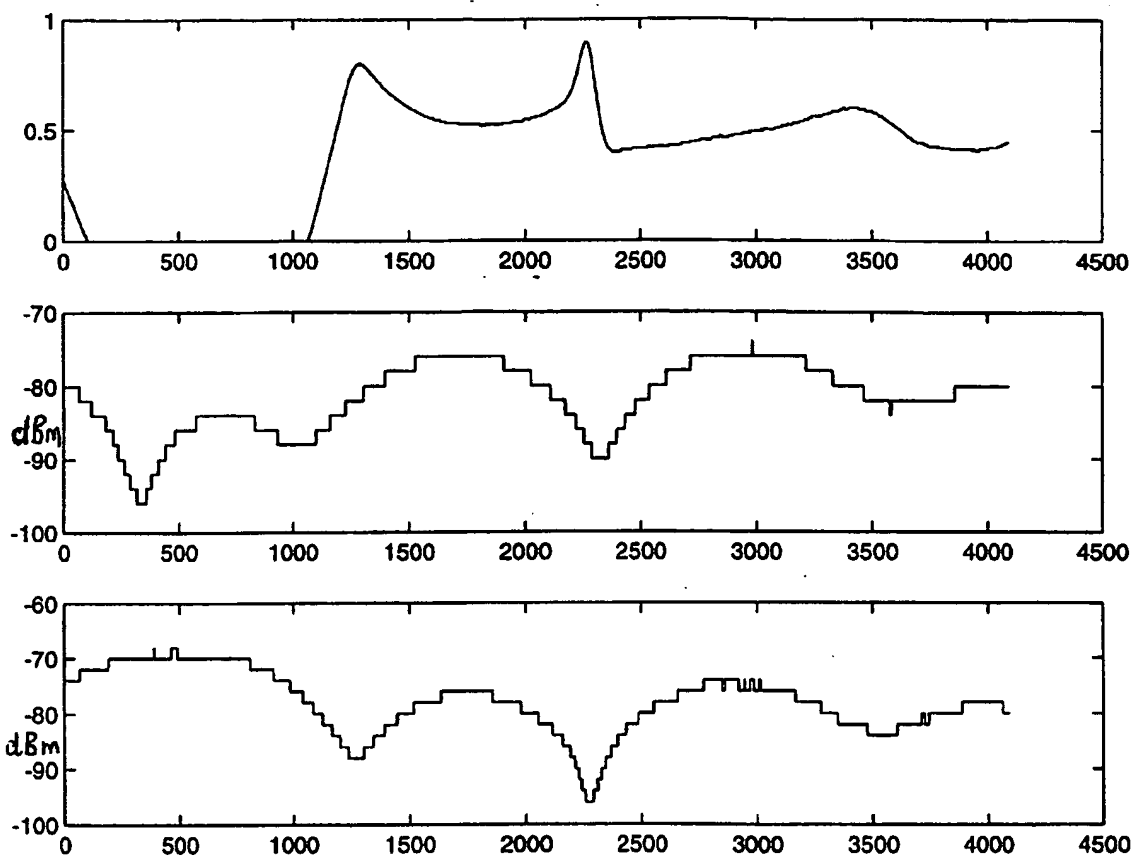

RSSID1
RSSID2
RXAD1
RXAD2
Serial Interface
Digital Filter
RSSI to dBm Converter
Adaptive DC Bias Compensation filter
Σ
α
1-α
Smart Combiner
Digital Filter
Polyphase Interpolation Filter
PLL
Integrate & Dump
Decision Device
RX Data
RX Clock
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48

Fig. 3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4000
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dBm
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-100
-60
-70
-80
dBm
-90
-100

FIG 4